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190125

**PATENT NUMBER and  
ISSUE DATE**

**U.S. UTILITY Patent Application**

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10053970	01/22/2002	438	48	2812	LONG, JR.

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36: 201

**\*\*CONTINUING DATA VERIFIED:**

**\*\* FOREIGN APPLICATIONS VERIFIED:**

GERMANY 101 02 432.0 01/19/2001

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>	
Foreign priority claimed		<input type="checkbox"/> yes <input type="checkbox"/> no	ATTORNEY DOCKET NO
35 USC 119 conditions met		<input type="checkbox"/> yes <input type="checkbox"/> no	MUH-12050
Verified and Acknowledged Examiners's initials			
TITLE : Test circuit for an analog measurement of bit line signals of ferroelectric memory cells			
U.S. DEPT. OF COMM. I.P.T. & T.M.-PTO-436L (Rev. 12-94)			

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G
ISSUE FEE			DRAWING	
Amount Due	Date Paid		Sheets Drwg.	Figa.Drwg.
		Primary Examiner		
			Application Examiner	
<input type="checkbox"/> TERMINAL <b>DISCLAIMER</b>		PREPARED FOR ISSUE		
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